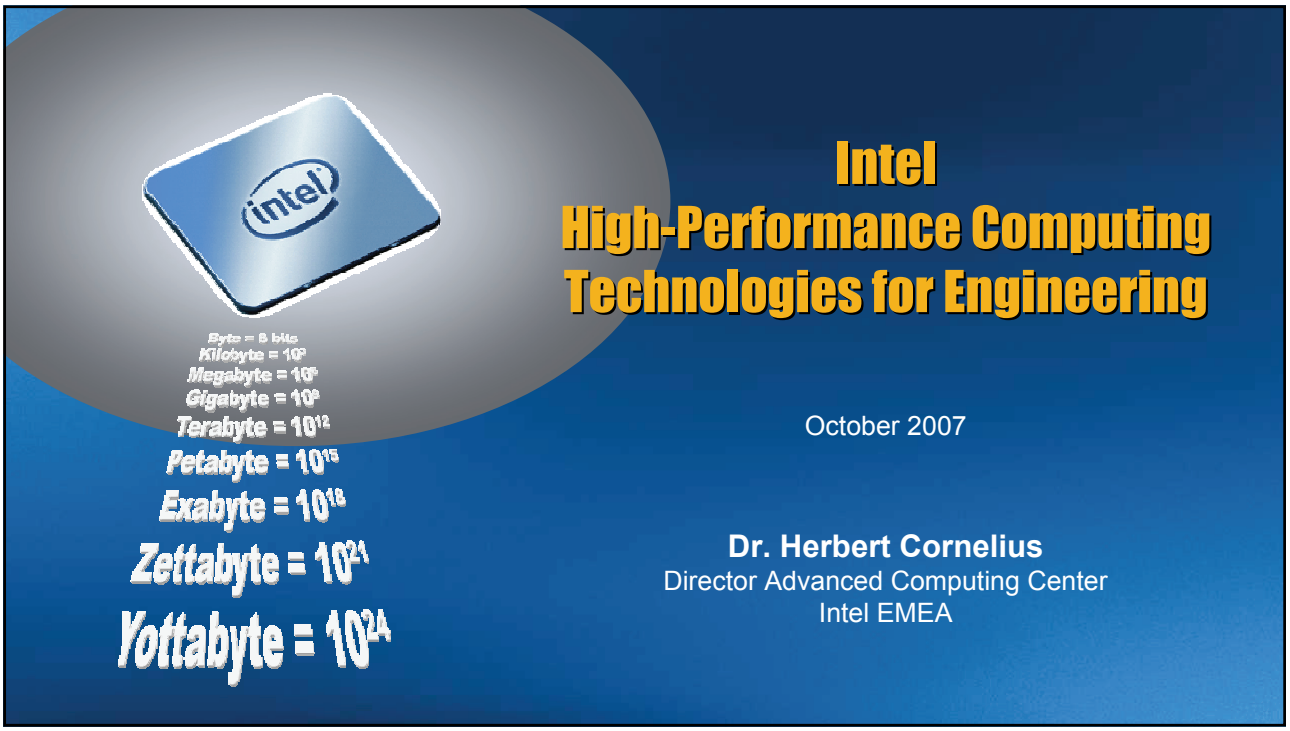
Intel High-Performance Computing

Technologies for Engineering

H. Cornelius

Intel GmbH



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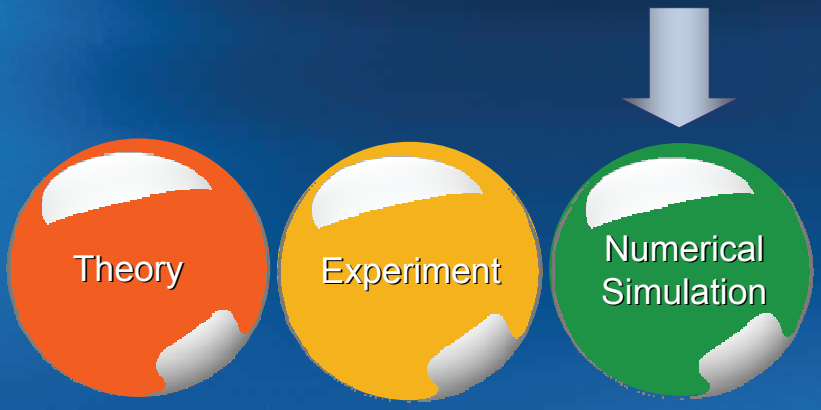
The Three Pillars of Science & Engineering



High-Performance Computing

GFLOPS [10^9] **TFLOPS** [10^{12}] **PFLOPS** [10^{15}]

yesterday … today … tomorrow …

From Supercomputers to Supercomputing …
A Strategic Investment

CAx Challenges

Shorten Design and Development Time

- Shorten time-to-market/money
- Better Products in all respect
- Reduce expensive and time consuming mechanical tests
- Reduce material (costs, weight, new)
- Optimize design specific features
- Keep competetive advantage

Solution:

High-Performance Computing (HPC)

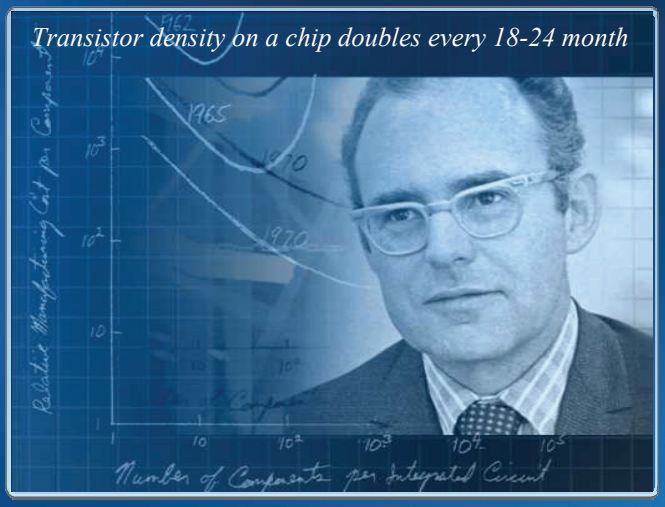
Numerical analysis and simulations on high-performance computer systems

- Increase capability and capacity
- More flexibiity and agility to changes
- More cost effective
- Simulate physical difficult tasks
- Better optimization within the design space

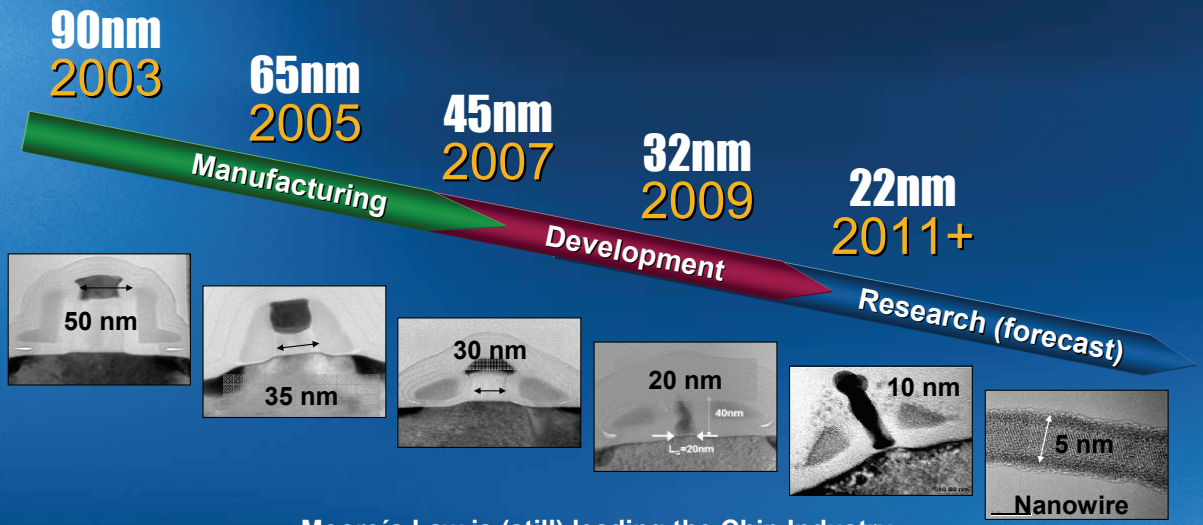
Changing the way CAD/CAE tools can be used

From serial to simultaneous workflows, reducing the time between an idea and a finished product using HPC Technologies

Moore´s Law is (still) Leading the Chip Industry



Ongoing Transistor Miniaturization

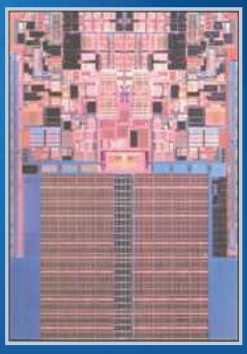


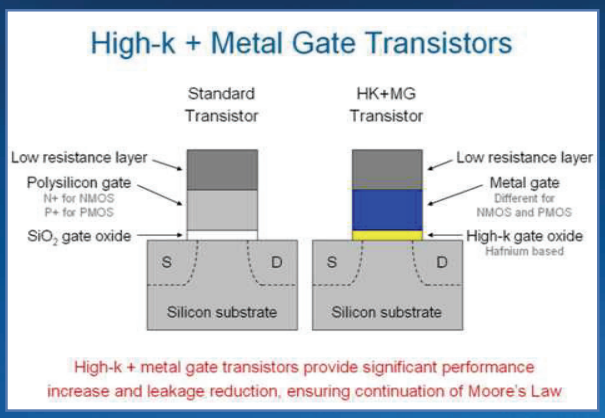
Moore´s Law is (still) leading the Chip Industry

Future options subject to change; Source: Intel

45nm Volume Manufacturing in 2007

Penryn Die Photo





Higher Performance with lower Power Consumption

Evolving Value Proposition

1960s-1980s

PERFORMANCE

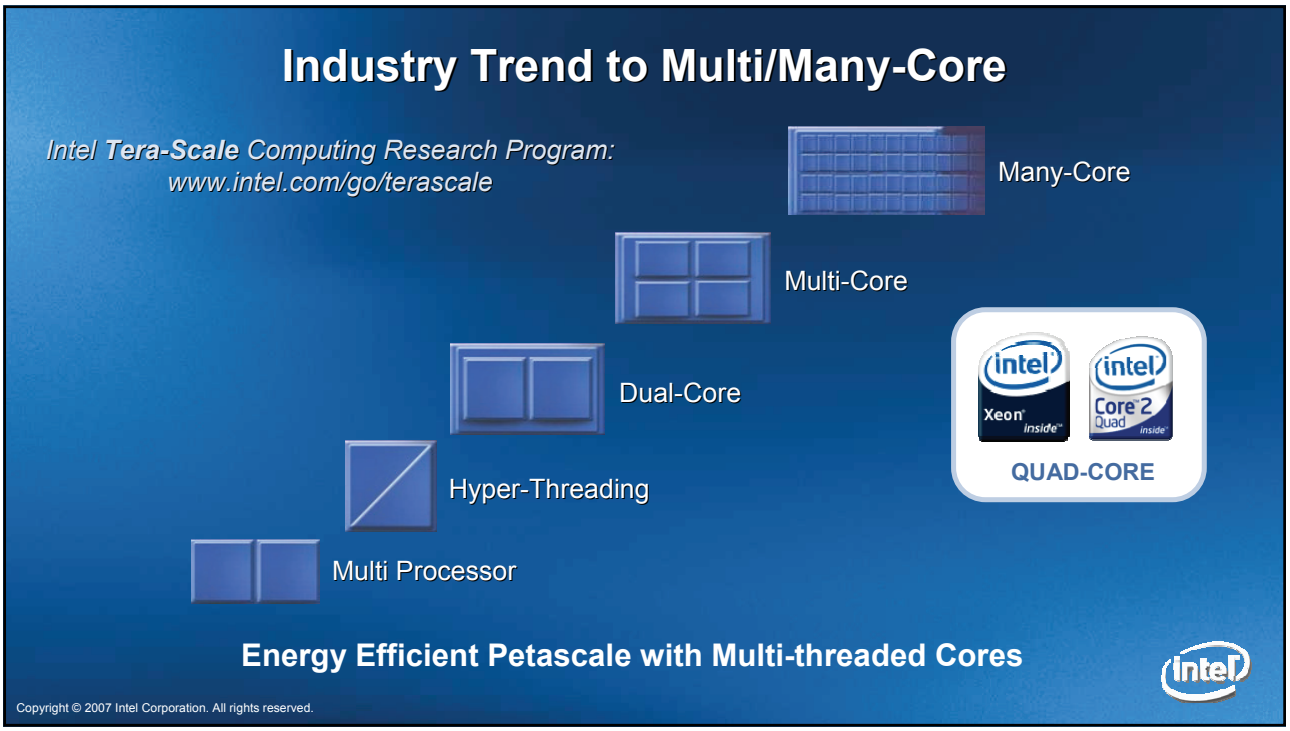
1990s

PRICE/PERFORMANCE

2000s

PRICE/PERFORMANCE/WATT

All Segments: HANDHELDS → CLIENTS → SERVERS → HPC


Industry Trend to Multi/Many-Core
Intel Tera-Scale Computing Research Program:
www.intel.com/go/terascale
Many-Core
Multi-Core
Dual-Core
Hyper-Threading
Multi Processor
QUAD-CORE
Energy Efficient Petascale with Multi-threaded Cores
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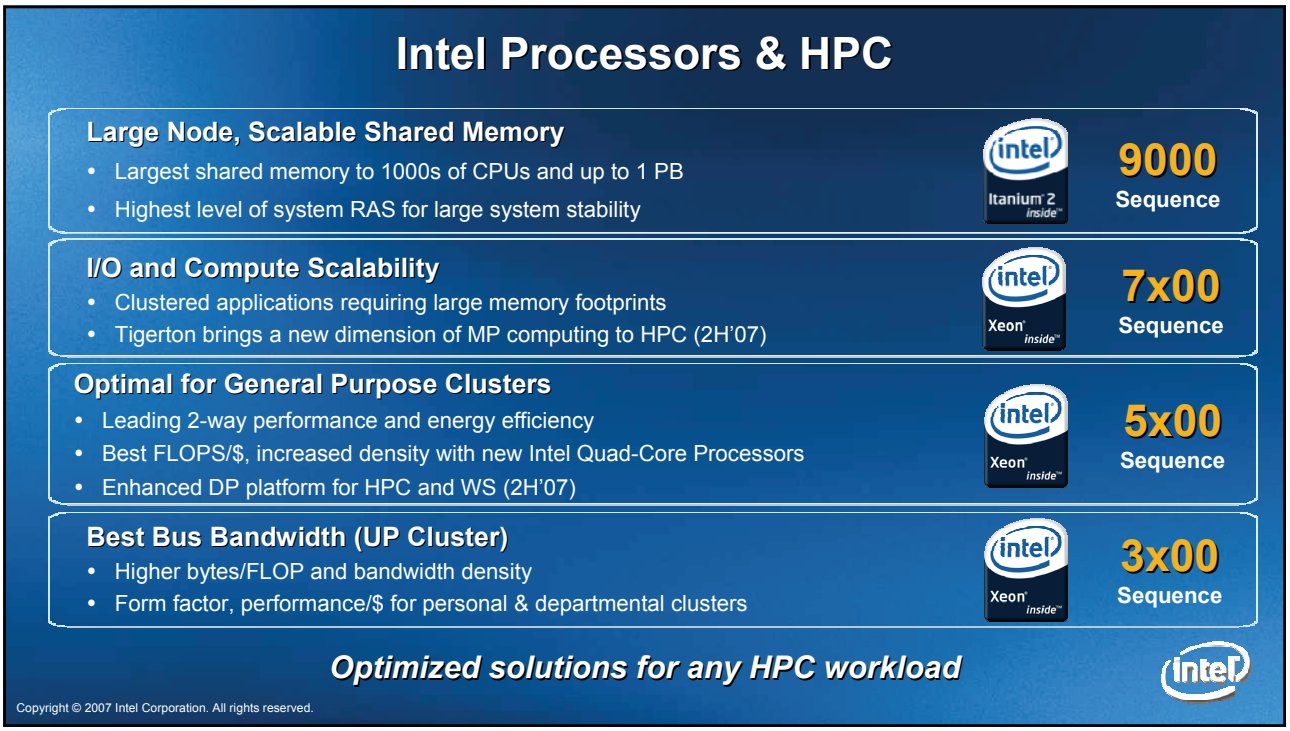
Intel Processors & HPC
Large Node, Scalable Shared Memory
• Largest shared memory to 1000s of CPUs and up to 1 PB
• Highest level of system RAS for large system stability
9000 Sequence
I/O and Compute Scalability
• Clustered applications requiring large memory footprints
• Tigerton brings a new dimension of MP computing to HPC (2H'07)
7x00 Sequence
Optimal for General Purpose Clusters
• Leading 2-way performance and energy efficiency
• Best FLOPS/$, increased density with new Intel Quad-Core Processors
• Enhanced DP platform for HPC and WS (2H'07)
5x00 Sequence
Best Bus Bandwidth (UP Cluster)
• Higher bytes/FLOP and bandwidth density
• Form factor, performance/$ for personal & departmental clusters
3x00 Sequence
Optimized solutions for any HPC workload
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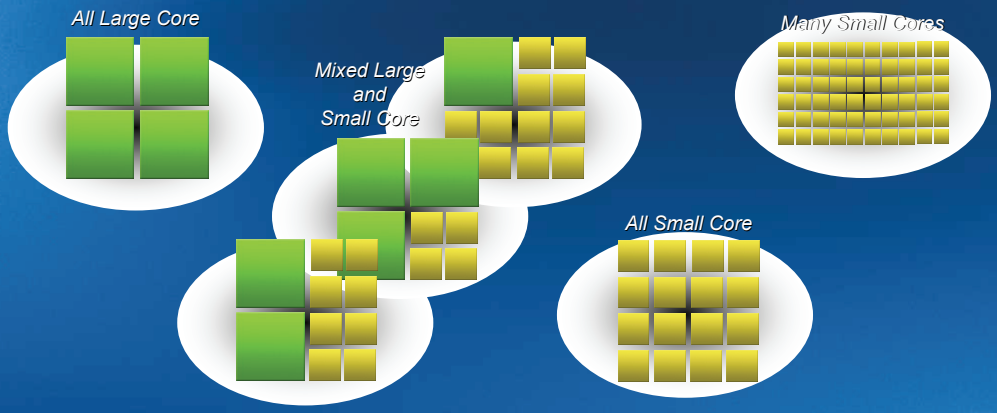
Multi-Threaded Cores

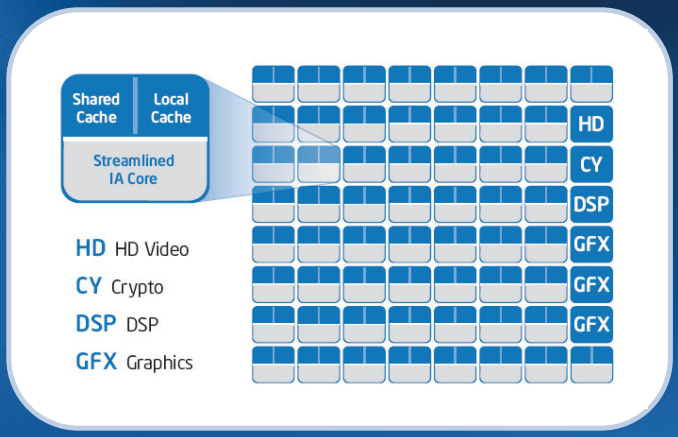
*Intel **Tera-Scale** Computing Research Program: www.intel.com/go/terascale*



Energy Efficient Petascale with Multi-threaded Cores

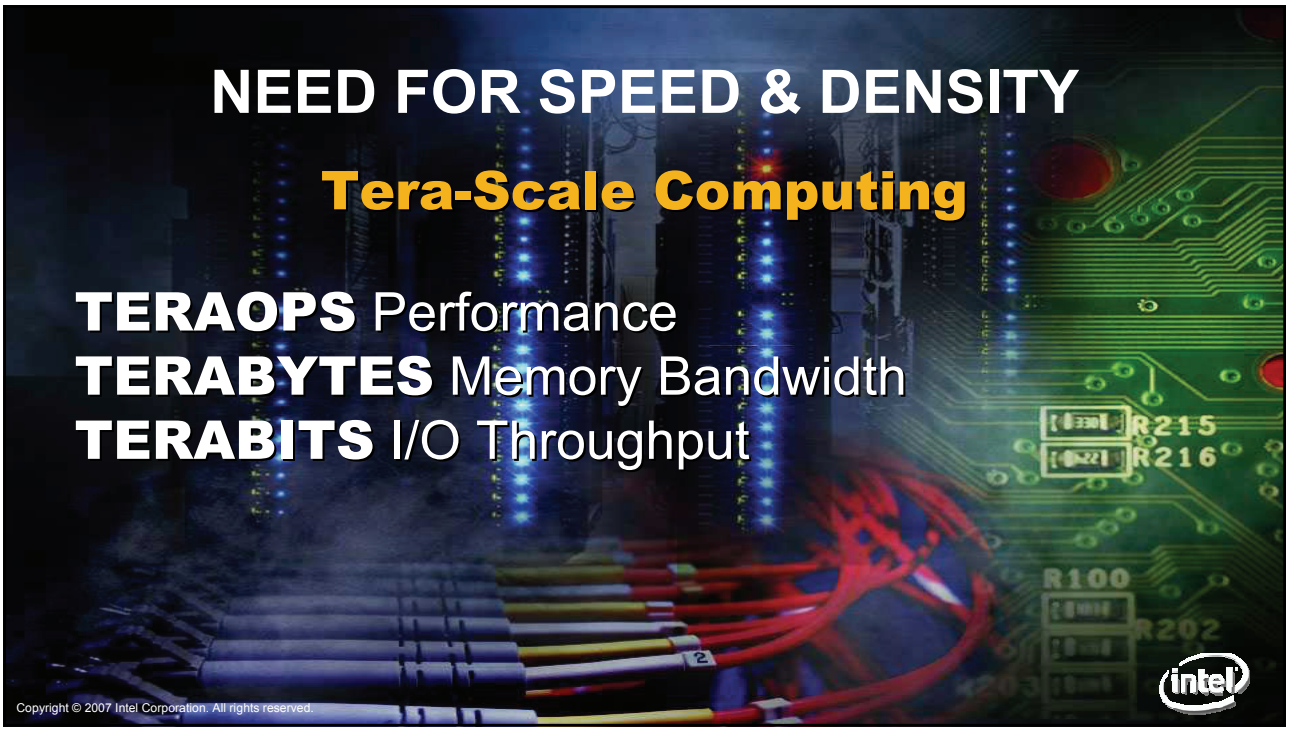
Note: the above pictures don't represent any current or future Intel products

Multi/Many-Core Chip Research



Future tera-scale chips could use an array of tens to hundreds of cores with reconfigurable caches, as well as special-purpose hardware accelerators utilizing a scalable on-die interconnect fabric.

All plans, products, dates, and figures are preliminary and are subject to change without any notice.


NEED FOR SPEED & DENSITY
Tera-Scale Computing
TERAOPS Performance
TERABYTES Memory Bandwidth
TERABITS I/O Throughput
R215
R216
R100
R202
intel
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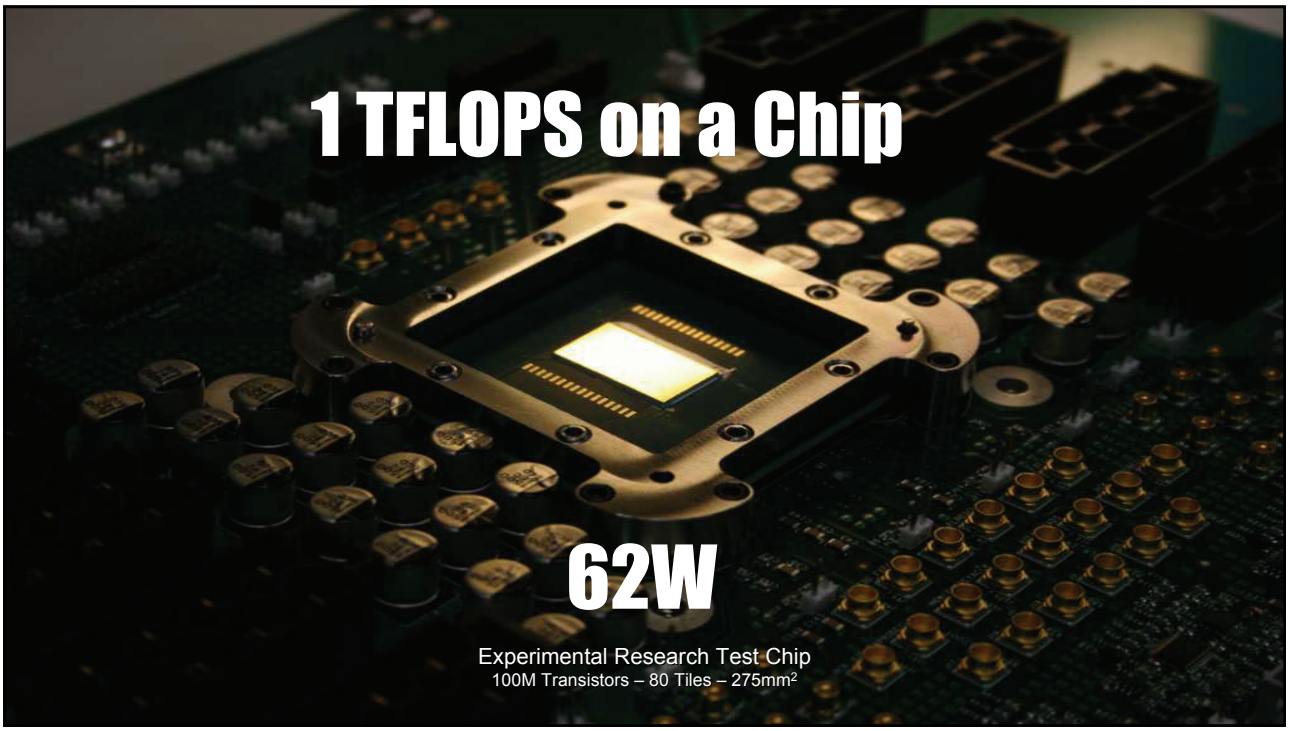
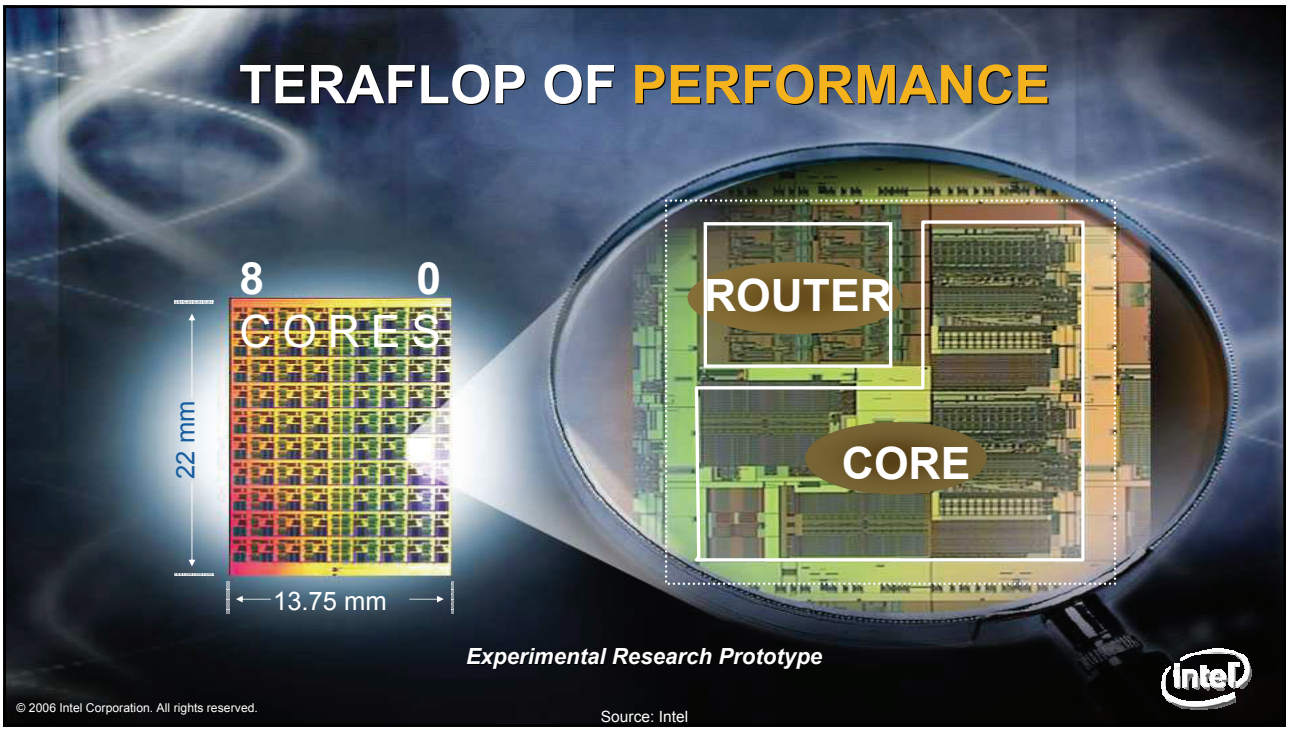
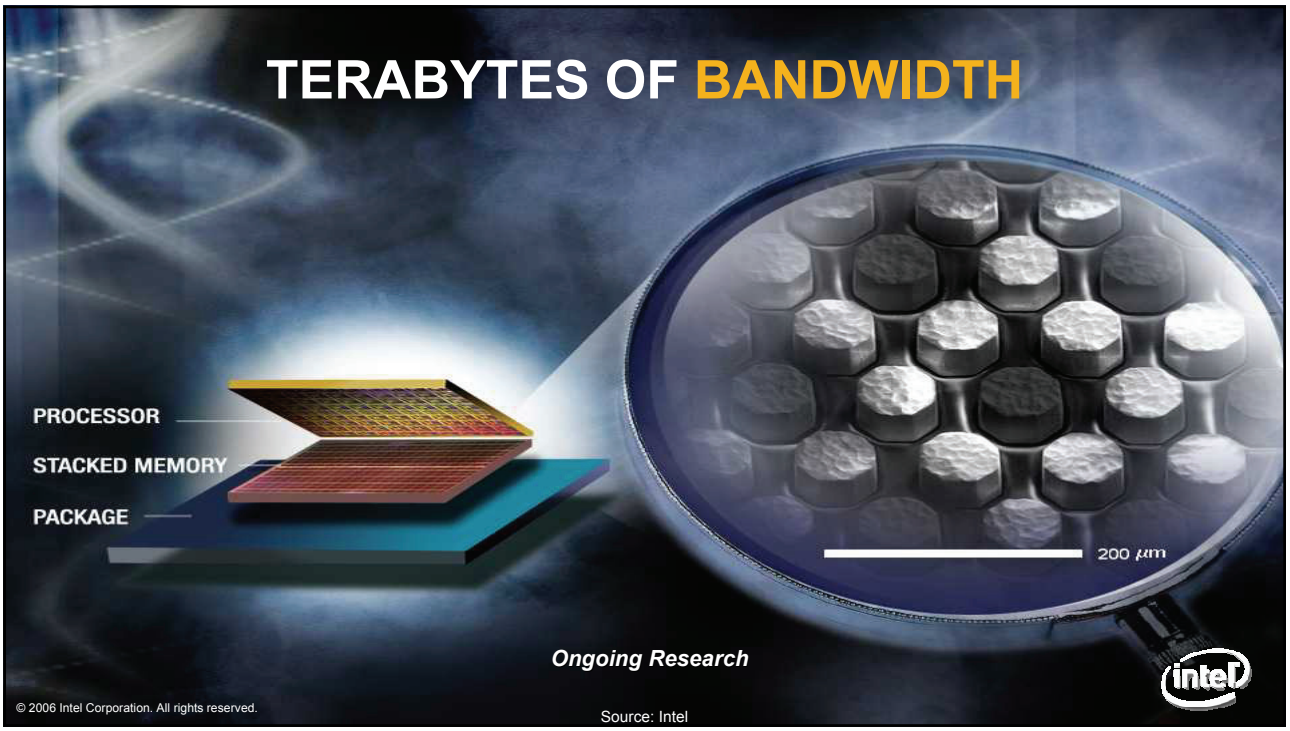
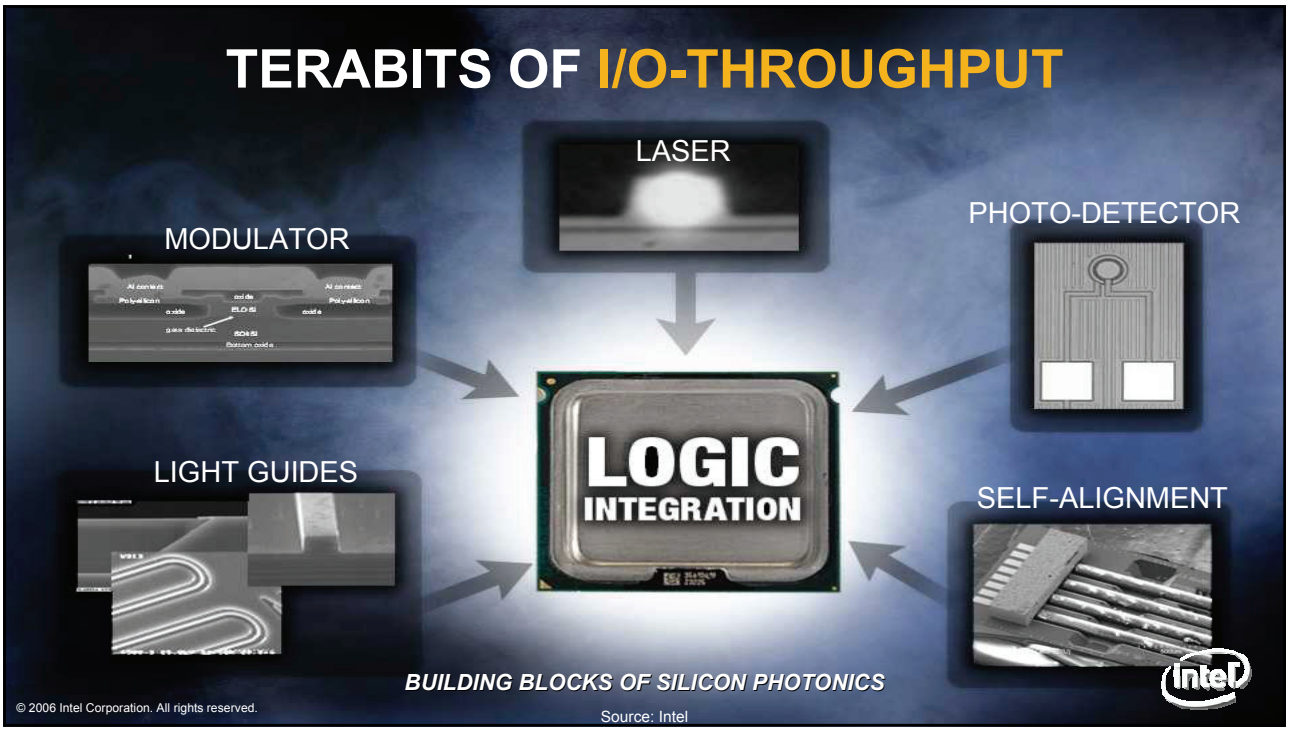

1 TFLOPS on a Chip
62W
Experimental Research Test Chip
100M Transistors – 80 Tiles – 275mm²






TERABITS OF I/O-THROUGHPUT
LASER
MODULATOR
PHOTO-DETECTOR
LOGIC INTEGRATION
LIGHT GUIDES
SELF-ALIGNMENT
BUILDING BLOCKS OF SILICON PHOTONICS
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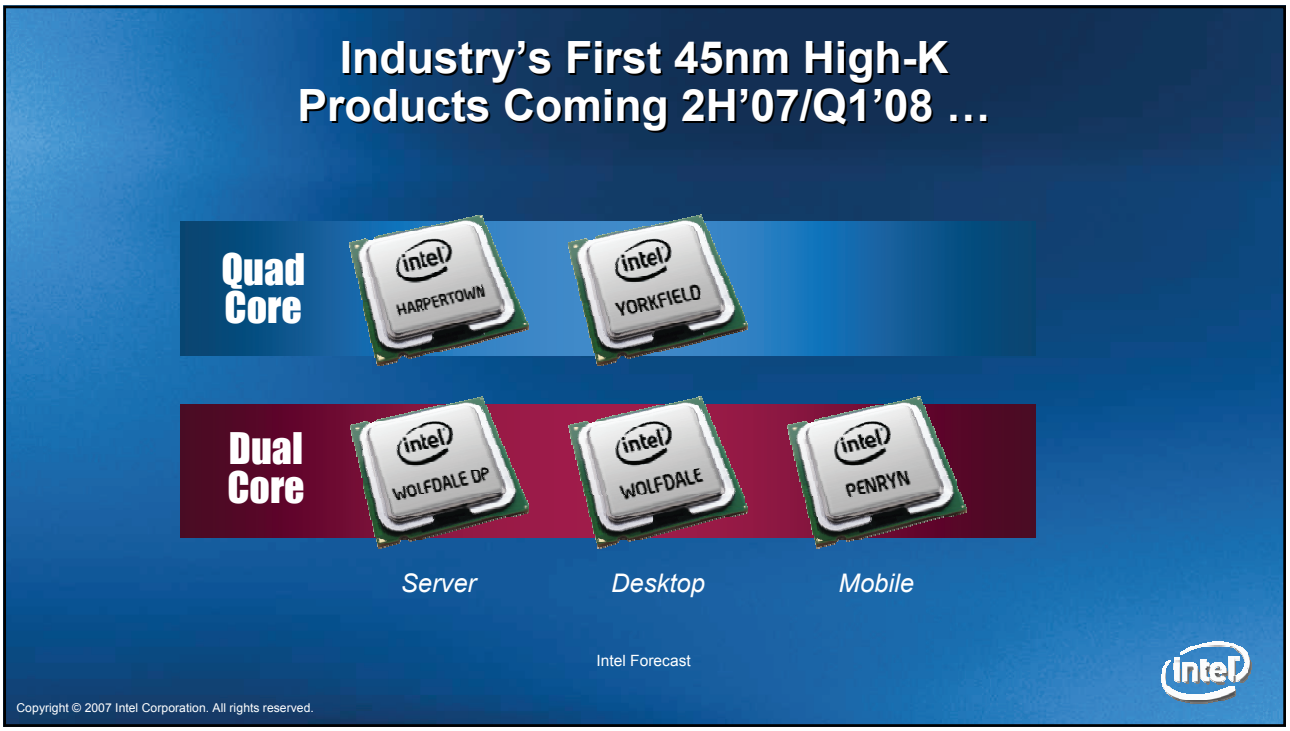
Source: Intel


Industry's First 45nm High-K Products Coming 2H'07/Q1'08 …
Quad Core
HARPERTOWN
YORKFIELD
Dual Core
WOLFDALE DP
WOLFDALE
PENRYN
Server
Desktop
Mobile
Intel Forecast
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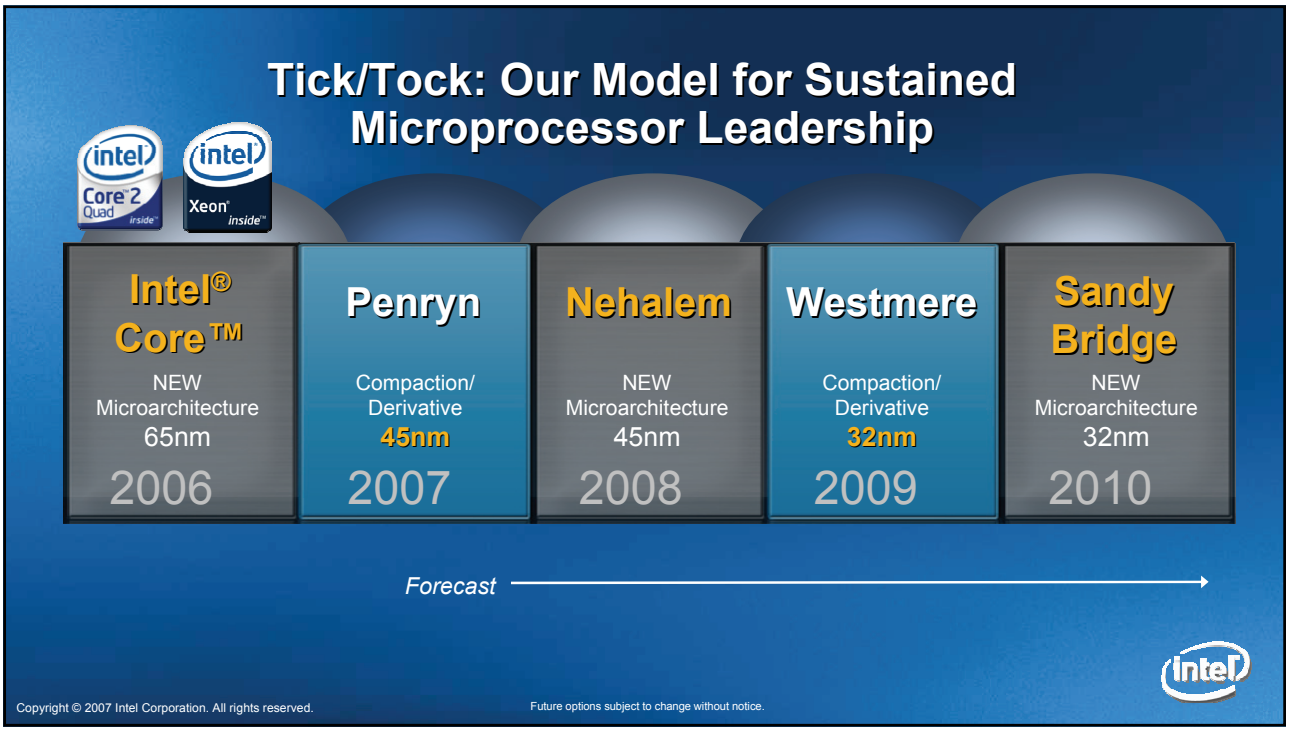

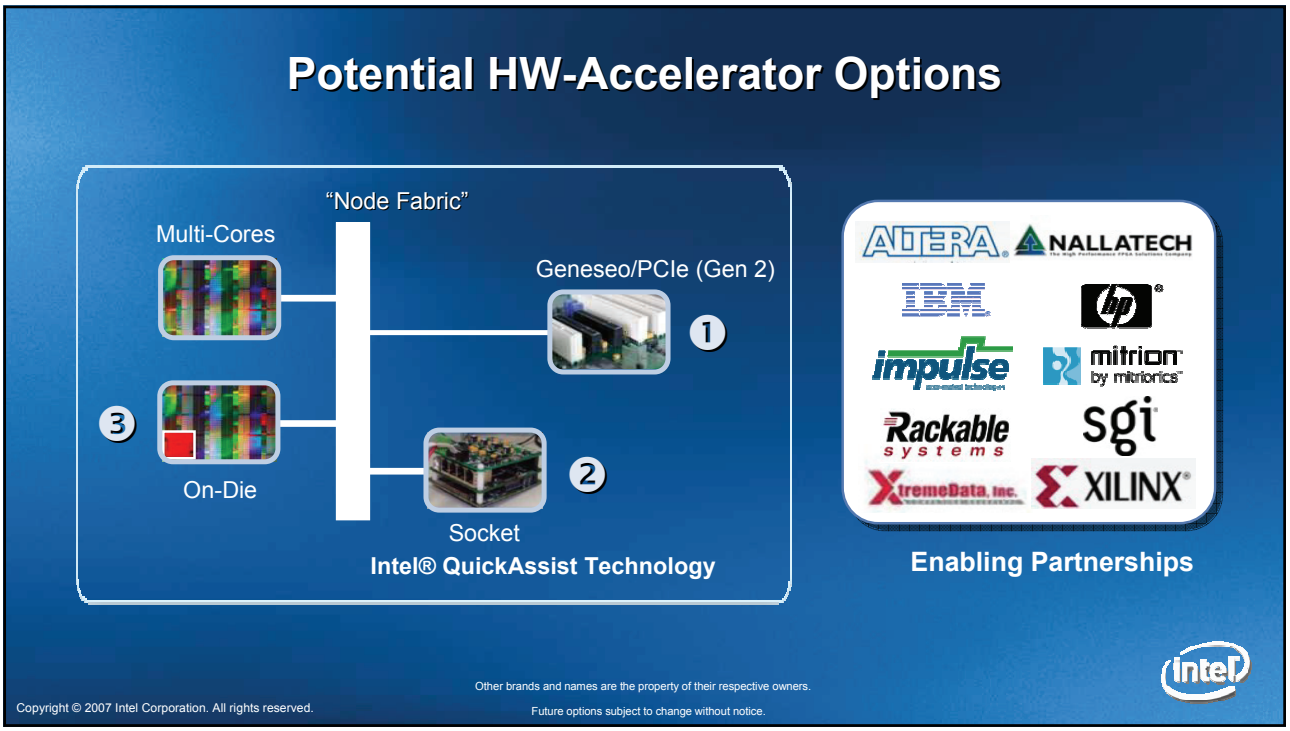

"Chip revolution poses problems for programmers: Software developers face a culture shock as they grapple with the next generation of microprocessors"

NewScientist, 10 March 2007

Intel's Software Tools and Support for HPC

Compilers

Performance Libraries

VTune™ Analyzers

Threading Tools

Cluster Tools

Intel® Cluster Toolkit

Intel® Thread Checker
Intel® Thread Profiler
Intel® Threading Building Blocks

ISN & ISC

ISS

Performance | Compatibility | Support | Productivity | Cross-Platform

www.intel.com/software

Levels of Parallelism
Intel SW Development Tools for HPC

	Serial Core Level	Multi-Core/SMP-Node level	Multi-Node Cluster Level	Grid Level
Programming Model Implementation	C/C++ FORTRAN95	Auto-Parallelization OpenMP* TBB	ClusterOpenMP Intel MPI	Intel GPE (UNICORE)
Correctness & Debugging	IDB	Thread Checker	Message Checker IDB-MPP	
Performance Libraries	MKL IPP	MKL IPP	Cluster MKL	
Performance Analysis	VTune™	VTune Thread Profiler	Trace Analyzer	

Intel® Software Tools for Parallelism

- **Architectural Analysis** — Visualization of parallel (threaded or MPI) application execution and communication behavior – give valuable insights for application architects and programmers
- **Introduce Parallelism** — Highly optimized OpenMP* and MPI library and run-time system for scalable solutions
  MKL threaded and distributed mathematical library
- **Confidence / Correctness** — Detecting actual and potential Threading and MPI programming and API issues - to address challenges unique to parallel programming
- **Optimize / Tune** — Valuable insights for performance and scalability tuning of threaded and MPI applications

Intel® Cluster Ready

A Program to make it easier for end users to buy, deploy and use clusters.

- Backed by reference implementations on Intel® Server Platforms (recipes)
  - Including tools to check compliance

A three-way collaboration between System Vendors/Integrators, Software Vendors, and Intel.

- Systems Vendors' (OEMs) and Integrators' solutions *certified* as compliant with the specification
  - May resell reference recipes or implement their own
- ISVs applications *registered* as compliant with the specification
  - Registered applications will run out-of-the box on any compliant cluster

More than a Cluster Solution Specification

Covering the Globe With Software R&D Labs

Over 50 Development Sites Across More Than 20 Countries

Conclusions

End-Users: The available compute power will continue to increase with flexible system architectures to meet the applications demand and requirements.

Software Vendors: Extract the available computational power via parallelization on all levels (multi-core, clusters) utilizing parallel software development tools for new and advanced functionality.

IT: Energy and cost efficient solutions continue to evolve providing the needed flexibility and business agility with improved capacity and capabilities.